Appendix 1: AFP Timing Electronics

This appendix includes an overview followed by schematics and pictures . Figure 1 shows a schematic overview of the proposed timing system, consisting of a quartz-based Cerenkov detector coupled to a microchannel plate photomultiplier tube (MCP-PMT), followed by the electronic elements that amplify, measure, and record the time of the event along with a stabilized reference clock signal.

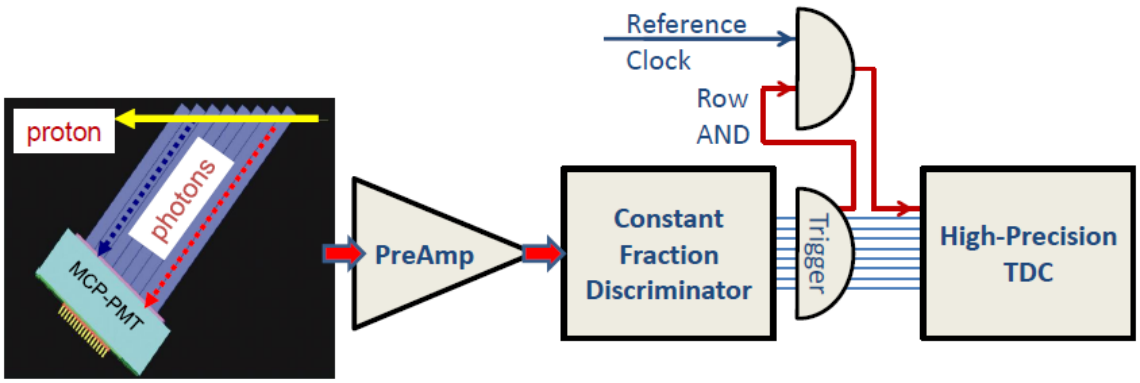
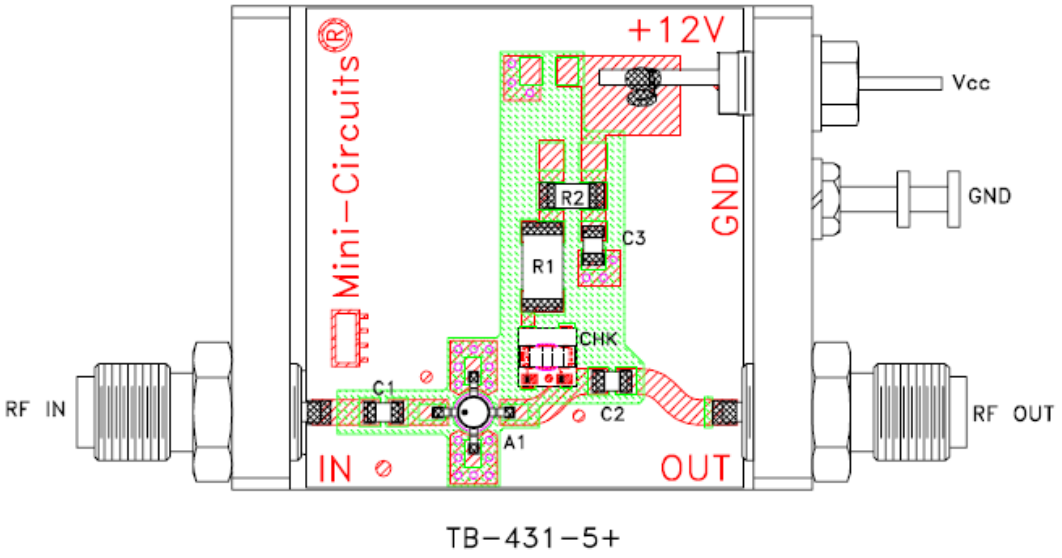


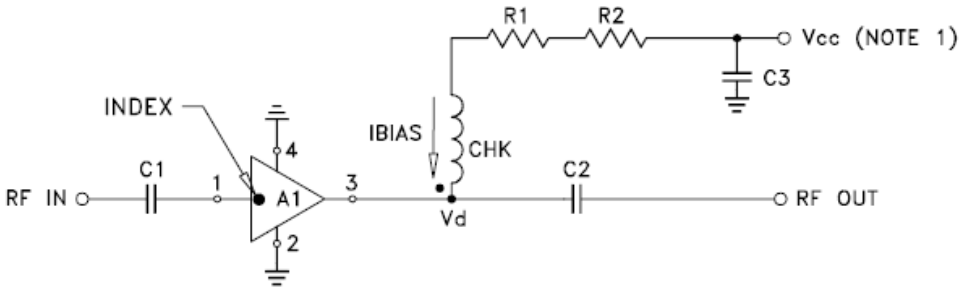
Figure 1: A schematic diagram of the AFP fast timing system.

The baseline QUARTIC detector consists of four rows of eight 5 mm x 5 mm quartz or fused silica bars ranging in length from about 8 to 12 cm and oriented at the average Cerenkov angle of 48^{o}. A proton that is sufficiently deflected from the beam axis will pass through a row of eight bars emitting Cerenkov photons, with those emitted in the appropriate azimuthal angular range accepted by the MCP-PMT. We have observed 10 to 15 pe's per bar in a reasonable time window. The MCP-PMT output pulse is processed by the read out system, which must digitize the pulse while maintaining the resolution for a single measurement at the desired level (~30 ps or better). For a 25 µm pore Photonis Planacon, we have obtained about 20 ps resolution in laser tests for this amount of light using a 405 nm pulsed laser with about 10 pe's. This includes the resolution of a constant fraction discriminator (CFD) that we have designed and built, which has better than 5 ps resolution, given at least 4 to 5 photoelectrons and an input signal of 300 mV or more. To obtain such a large signal while operating the PMT at low gain (<1x10^{5}) due to lifetime considerations, requires a high quality amplifier. We have designed and built a suitable pre-amplifier board based on the low noise, high bandwidth, high radiation-tolerant GALI-39+ amplifier (which is similar to the active component in Minicircuits amplifiers used in previous tests). The schematic for a single channel, including over-voltage protection is shown in Fig. 2, with a photograph of a prototype board in Fig. 3.

Coincidences of the CFD output signals will be used to form Level 1 triggers, which can range from a simple ``proton in detector'' trigger, to more sophisticated triggers that select mass bins (based on the distance of the proton from the beam), to complex triggers that correlate the

proton and calorimeter information. The trigger signal will also be used to gate the reference clock signal, which uses a phased-lock-loop feedback system to keep the jitter of the clock on the few ps scale. This gated clock signal will thus only be recorded for events with protons, avoiding the loss of information in the digitization stage that arises when the occupancy is too high. The gated CFD and timing signals are digitized by the HPTDC chip (high precision time-to-digital converter) which is incorporated into a board that will interface with the ATLAS read out system.





COMPONENT	VALUE
A1	ERA-5(+)
C1 (NOTE 4)	2400 pF
C2 (NOTE 4)	2400 pF
C3 (bypass)	0.1 uF
R1	110 Ohms, 0.75W
R2	0 Ohm, 0.25W
CHK	Mini-Circuits TCCH-80+

Figure 2: A schematic diagram of an amplifier channel.

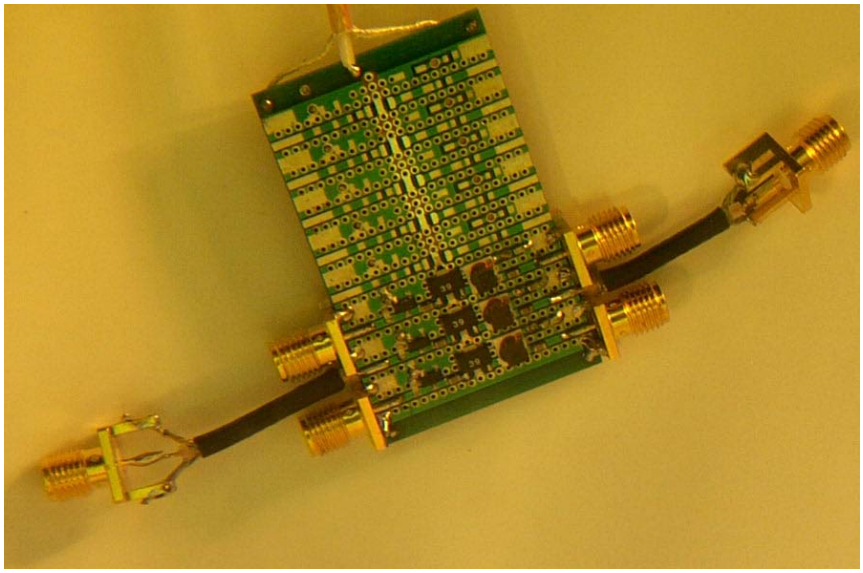


Figure 3: A photograph of a prototype 8 channel amplifier card, with 3 channels instrumented.

The CFD circuit was originally developed by University of Louvain, and had been modified by Alberta and Stony Brook. The layout of a single channel (mini-module) is shown in Fig. 4, with the corresponding photograph in Fig. 5

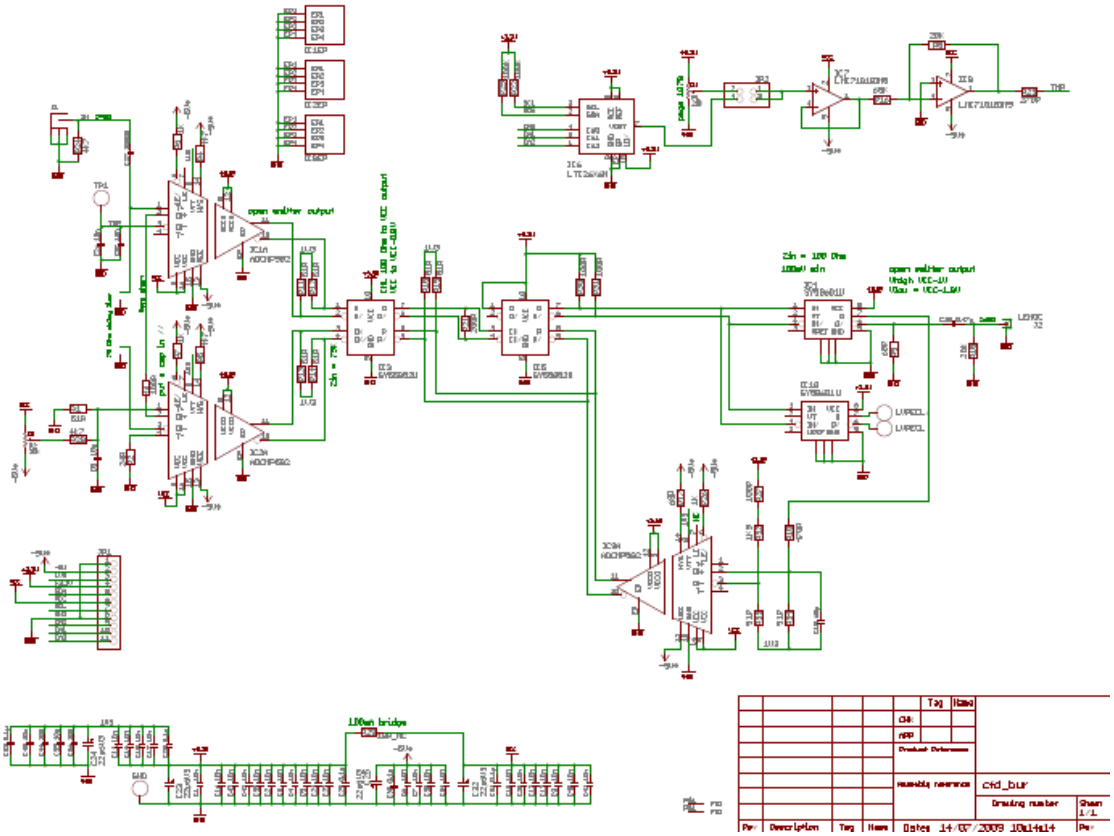


Figure 4: A schematic diagram of a CFD channel originally designed by Louvain.

Figure 5: A photograph of a single CFD channel board (minimodule).

Alberta has also adapted the original Louvain design of the motherboard NIM module (that houses and provides low voltage to eight CFD minimodules). In addition to a lemo output for debugging, the minimodules also provide an LVPECL output to the HPTDC board. This module, when fully populated with 8 CFD mini modules will dissipate about 15 Watts, so the NIM crate should be well ventilated. A schematic diagram and photographs of the CFD motherboard is shown in Fig. 6.

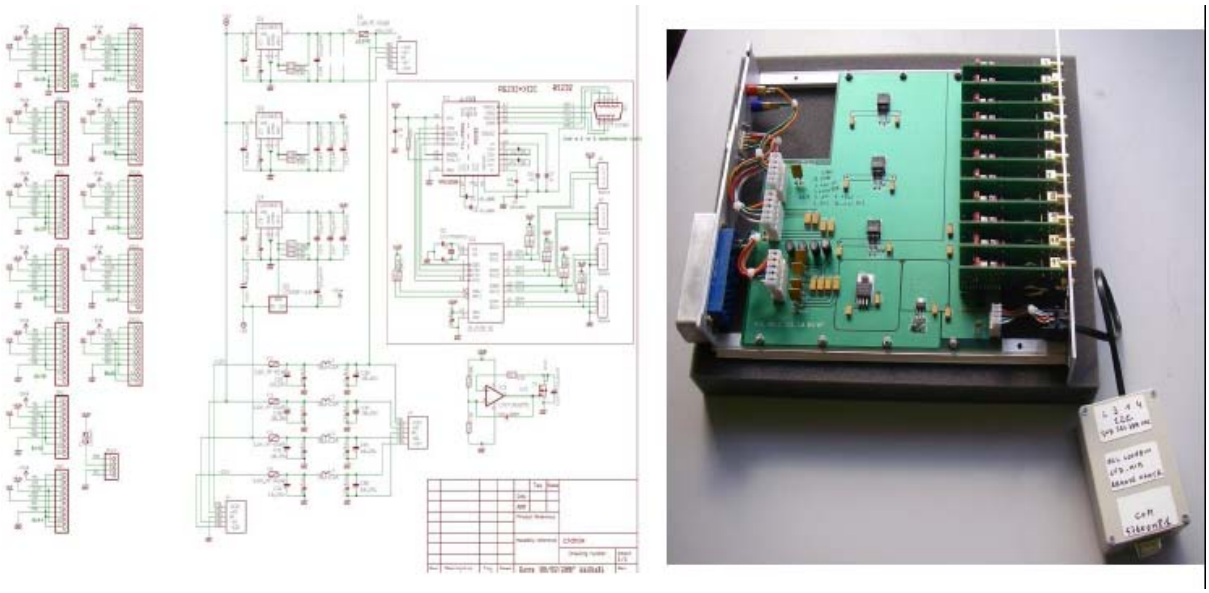


Figure 6: A schematic and a photograph of the NIM CFD module motherboard.

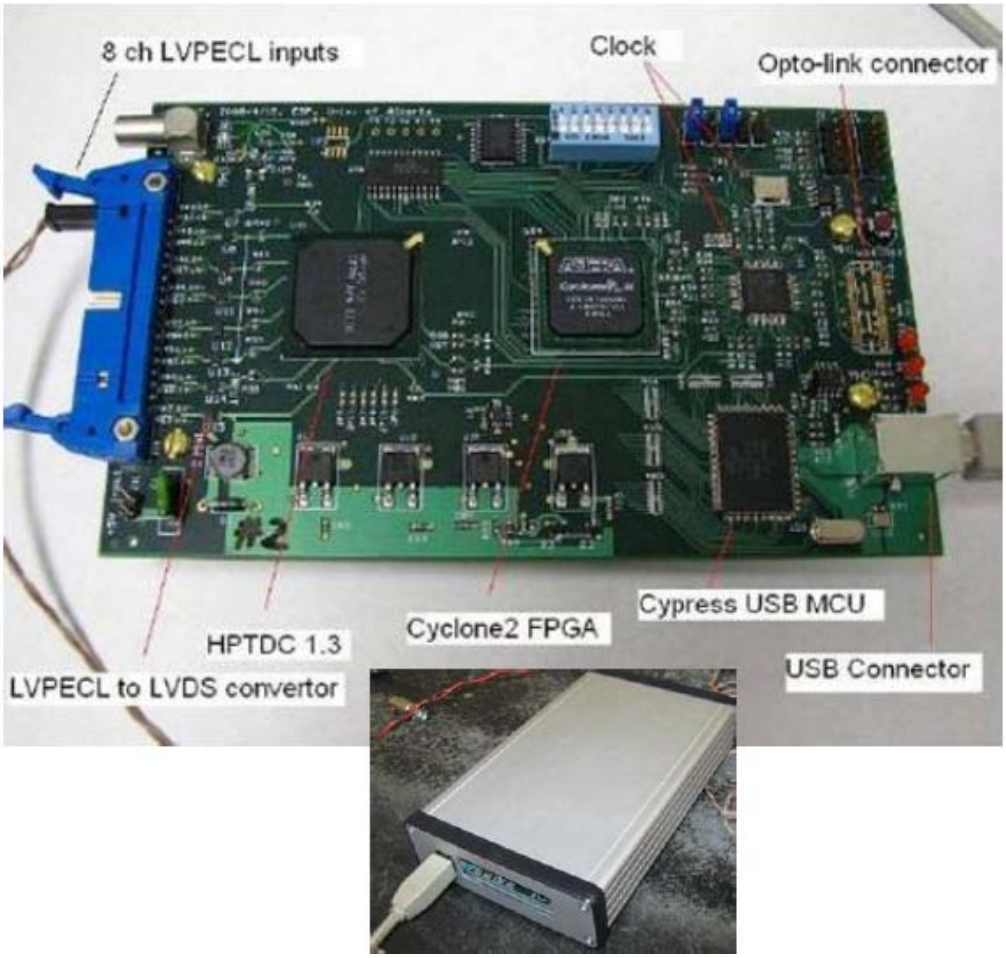


Figure 7: A photograph of the prototype Albeta HPTDC board, and the standalone box that contains the board.

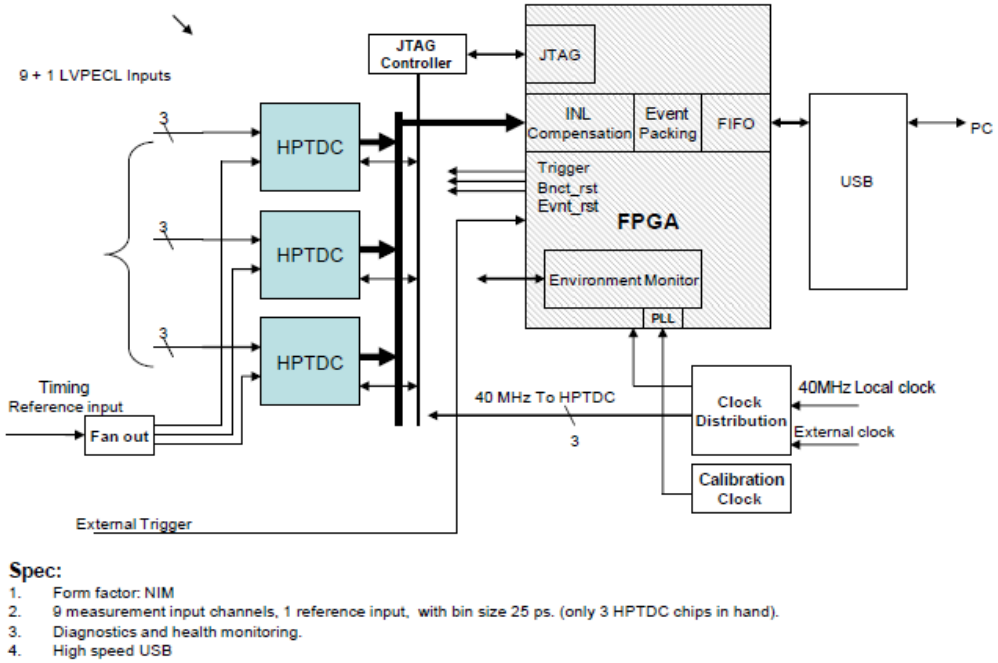


Figure 8: A sketch of the the three HPTDC chip version of the Albeta HPTDC board. The schematics are included in Appendix2.

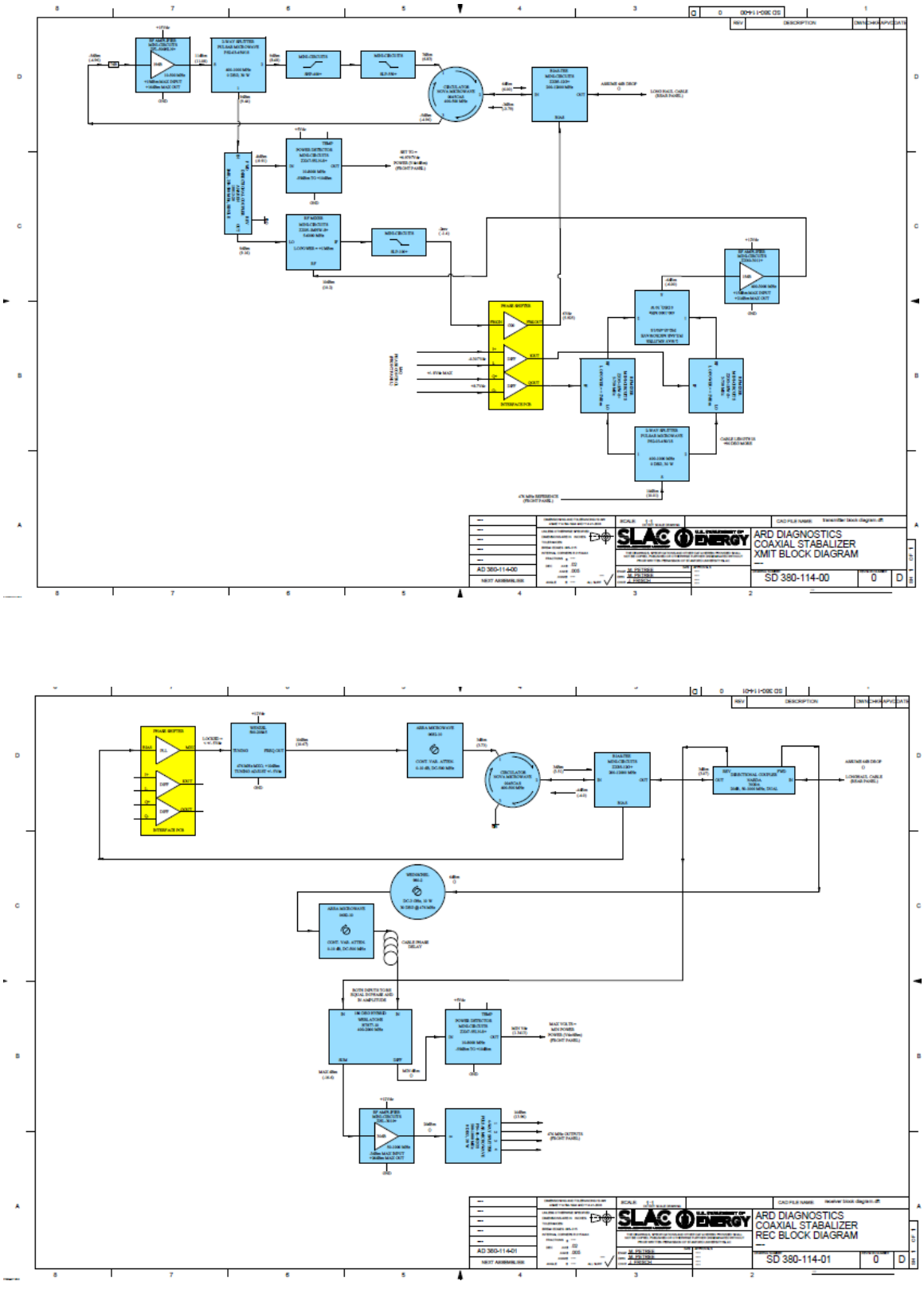


Figure 9: A schematic of the reference clock circuit designed at SLAC.