AFP: Fast Timing System R&D Plans

As discussed in the Technical Proposal, we have developed a proof-of-concept of the fast timing detector system capable of 10 to 20 ps resolution, depending on the number of channels employed. There is still quite a bit of R&D required, however, to get to a full system prototype that is capable of being installed in mid-2013. This R&D falls into two main categories: 1) fairly routine refinements of the system, involving the detector layout and electronics chain, which are clearly doable and just need to be completed; 2) long term stability issues involving micro-channel plate PMT lifetime, assessing the radiation hardness of components, and developing a system with sufficient radiation tolerance to operate for a year or more without intervention.

The location at 220 m from the ATLAS IP has expected radiation levels around 2 10^{11} neutron-equivalent per cm^2 at the beam pipe (this corresponds to a luminosity of 100 fb^{-1}), decreasing with distance. At the position of the detector, MCP-PMT, and the pre-amplifier, the levels are expected to be 10^{10} or less. This leads to an integrated dose on the order of $\sim$ 200 Grays for a luminosity of 100 fb^{-1}. We expect to install the remainder of the timing electronics in the alcove at 240 m, where the expected dose is of the order of 0.1 to 1 Gray. We plan to analyze radiation monitoring data as the luminosity increases, to develop a more thorough understanding of the radiation environment of the detector, and then plan irradiation studies of the various components in summer of 2012.

An overview of the goals of the remaining R&D and timescales involved for both of these development categories are discussed below in the context of the three main components of the fast timing system: the detector, the photo-sensor, and the electronics.

1 Detector R&D

The detector development effort to date has demonstrated that fused silica bars produce enough light within a reasonable time range to meet our detector resolution goals. Prototype tests have generally been one row (8 channels) of 5 mm $\times$ 5 mm pixels, while the final detector design needs to be refined to incorporate full acceptance out to 20 to 25 mm from the beam. Another development issue is reducing the width of detector bins close to the beam, while maintaining the same MCP-PMT pixel size to equalize the rate per unit area. Not only would this improve the multi-proton timing capability (which becomes important at high luminosity, where the overlap background is worst), but it would also reduce the rate and lifetime requirements of the MCP-PMT, which are dominated by the pixels closest to the beam. Two offset quartz bar detectors could be used to avoid "cracks" (regions of poor acceptance), and reduce the bin size near the beam, with the desired variable bin size being achieved by combining successively more pixels for bins further from the beam. Variable detector bin size could, however, most easily be achieved using quartz fibers instead of quartz bars, where the quartz fibers could be grouped into different pixels as desired. This option is being explored primarily by Giessen, who have built a quartz fiber prototype detector. Alberta also have started to explore quartz fiber options, producing a few single channel composite quartz bars (composed of several different fiber diameters). A hybrid design where quartz bars are fed into clear light guide fibers is also conceivable. The final detector refinement under consideration is employing a low pass filter. Preliminary results indicate this is somewhat beneficial to the overall resolution, where the narrower wavelength range reduces the resolution broadening from color dispersion more than the decreased amount of light increases it.

1.1 Goals and timescales for detector R&D

The final detector R&D thus focusses on preparing a full detector prototype with variable bin size.

1. **Goal:** Use test beam data to choose between quartz bars and fibers. **Timescale:** Summer/Fall 2011
2. **Goal:** Determine optimal pixel size to equalize rate. **Timescale:** Fall 2011
3. **Goal:** Finalize detector layout assuming Photonis MCP-PMT. **Timescale:** Dec. 2011
4. **Goal:** Construct detector prototype. **Timescale:** April 2012
5. **Goal:** Detector radiation tests. **Timescale:** June 2012
6. **Goal:** Validate final detector in test beam. **Timescale:** Aug. 2012

Outlook: This task is straight forward and should be accomplished with little technical or schedule risk given modest funds. Note using a different photo-sensor from the default Photonis Planacon would lead to modest changes in the layout, and require a new prototype design.

2 Photo-sensor R&D

The primary type of photo-sensor being considered is the MCP-PMT, although Giessen and CMS are investigating silicon photomultipliers (SiPM) as a possible alternative to the MCP-PMT (the idea would be to use a QUARTIC-like design with SiPMs at end of the quartz bars instead of MCP-PMTs). A key issue for the MCP-PMT approach is the degradation of the quantum efficiency of the photocathode from back-scattered positive ions. Assuming 10 pe's/0.33 cm^2 pixel and a gain of 5×10^4, we get a current of about 0.25 $\mu A/cm^2$ per MHz proton rate. To estimate the proton rate, we use a worst case 2014 scenario with a constant level of 25 interactions/crossing at a bunch spacing of 50 ns. With detectors positioned at 2.0 mm from the beam, PYTHIA gives a 1.7% chance/interaction of having one or more protons in our acceptance. Applying Poisson statistics, we expect .346 protons/bunch which gives 0.173 protons per bunch per detector. A 20 MHz bunch rate/detector yields a 3.5 MHz proton rate/side. Half of these protons are within the 5 mm pixel closest to the beam; an optimized design could lower this by another factor of two, yielding a proton rate of less than 1 MHz, which corresponds to about 2.5 C/cm^2 integrated charge/year during Stage 1 operations. For Stage 2 operations assuming 35 interactions per crossing at 25 nsec bunch spacing gives 2.5 MHz/pixel and an integrated annual charge of about 6 C/cm^2. As discussed in the TP, the standard approach to improving the lifetime is to add an ion barrier, a thin film that inhibits the flow of positive ions, on top of or between the MCP's. Recent results with the Hamamatsu SL10 indicate that the lifetime is stable to several C/cm^2 which should already be acceptable for Stage 1. UTA is working on a Small Business proposal with Arradiance and Photonis, incorporating atomic layer deposition (ALD) coated MCP's into the Photonis Planacon, and evaluating the lifetime. Initial results are very promising, with lifetime on the same scale as the Hamamatsu test. In principle, the combination of an ion barrier and ALD coating could provide the life time improvement required for Stage 2. We are also collaborating with Photek, another MCP-PMT vendor that is interested in making long life MCP-PMT's using a more robust "solar blind" photocathode, and could combine this with the other lifetime improvements into an ultra long life MCP-PMT. We note that the solar blind photocathode should only give a minor reduction in light, since

Cerenkov radiation is peaked in the UV, and in fact, we are planning to put a low wavelength pass filter on the detector in any case.

2.1 Goals and timescales for photo-sensor R&D

This R&D effort is focussed on developing a high-rate long-life MCP-PMT sufficient for Stage 1 and 2, where the Stage 1 device needs to be ready for use in a full timing system test beam in Summer 2013, while the Stage 2 device would not be needed until 2016 or so.

1. **Goal:** Lifetime tests on a first generation improved Photonis MCP-PMT. These tests are currently in progress with a goal of a few C/cm^2. **Timescale:** August 2011
2. **Goal:** Lifetime tests on a second generation improved Photonis MCP-PMT (optimized ALD coating) with a goal of 5 C/cm^2. **Timescale:** December 2011
3. **Goal:** Lifetime tests on a third generation improved Photonis MCP-PMT (further optimized ALD coating, possibly including resistive layer) with a goal of 10 C/cm^2. Test a Hamamatsu tube and a hybrid Photek tube with ALD and ion barrier that could attain 20–30 C/cm^2. **Timescale:** December 2012
4. **Goal:** SiPM irradiation tests. **Timescale:** July 2012
5. **Goal:** MCP-PMT irradiation tests. **Timescale:** summer 2012/2013 for second/third generation
6. **Goal:** Further development of an ultra long life hybrid tube combining various upgrades, perhaps capable of $>$ 30 C/cm^2. **Timescale:** July 2014

Outlook: This task is on the critical path. If the NSF Phase II SBIR proposal is funded as anticipated, this would lead to the second and third generation Photonis MCP-PMT, which would incorporate optimized ALD-coated MCP's. There is a very good chance that this task will converge, but there is some scheduler and technical risk. The Photek development effort may be necessary for Stage 2–unfortunately, there are currently no funds for this. Modest R&D funds to commission Photek development and to purchase a Hamamatsu prototype, would be most welcome. Note the MCP-PMT development is coupled with the detector from the point of view of the pixel size, so if a different MCP-PMT or other type of photo-sensor is used, then the exact details of the detector layout will have to be modified.

3 Electronics R&D

We have developed and tested a prototype of the full electronics chain which consists of pre-amplifiers, constant fraction discriminators, trigger, and a high precision time-to-digital converters (HPTDC) as shown in the schematic overview in Fig. 1. The final component is the reference clock, which has been developed by SLAC.

Here we outline the electronics R&D still in progress. First we are developing an amplifier PCB board to replace the discrete components. A prototype has recently been completed and is being tested. The existing Constant Fraction Discriminator (ALCFD) works well, but it would be beneficial to have programmable gain (or adjustable attenuation) for optimal CFD performance. We will also explore the feasibility of adding a low resolution 8 bit ADC for monitoring the MCP-PMT gain, and perhaps correcting for small or pathological pulses. We plan to route the fast timing signals to the motherboard where the fast trigger circuitry will

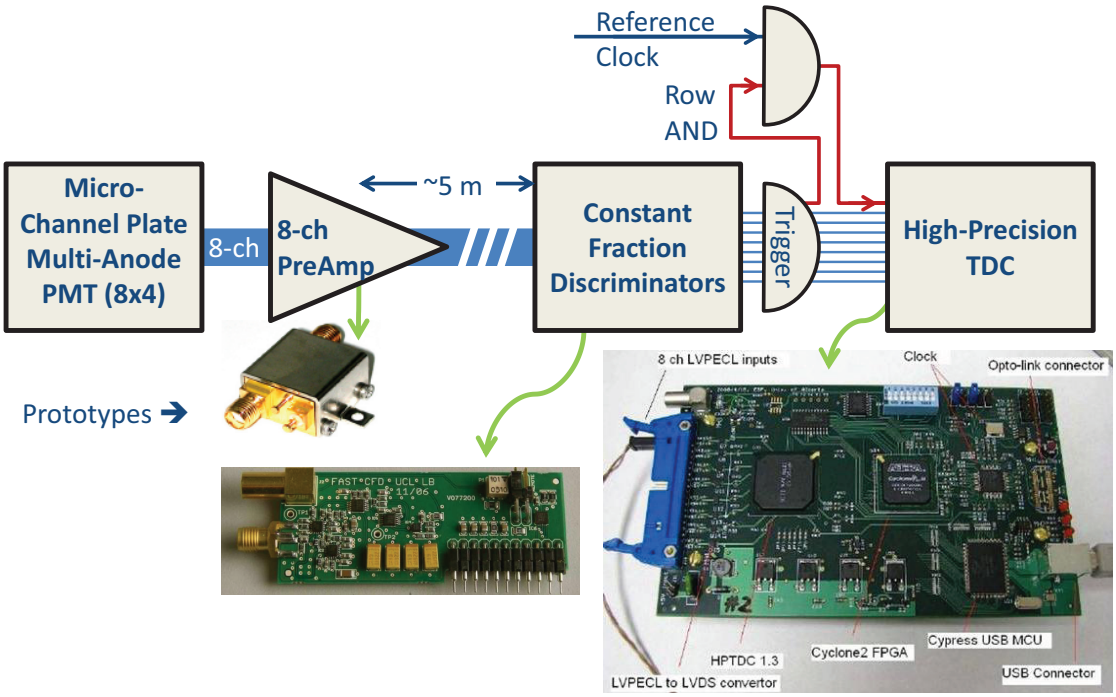

Figure 1: A schematic diagram of the electronics chain described in the text. The photographs show a low noise Minicircuits ZX60 pre-amplifier, a constant fraction discriminator daughter board, and the HPTDC board used in laser and beam tests.

be implemented. The fast signals, the reference time signal, and the row trigger signal will be transmitted via the analog backplane to the time digitizer modules.

A dedicated VME trigger module will form the OR of all row triggers into a single-arm master trigger for transmission to the ATLAS central trigger processor. When a trigger occurs, the high-precision reference clock signal will be passed along with the row signals for digitization. The trigger logic must preserve the channel timing resolution and introduce a channel jitter of less than 5 ps. The trigger logic, although quite straight-forward remains to be designed and implemented.

We have developed and tested a single chip HPTDC board, but are in the process of designing it to use 3 HPTDC chips to account for the switch from a 40 to 80 MHz internal clock as described in the TP, which limits the chip to four useful channels, one of which is dedicated to the clock signal. The interface of the HPTDC to the ATLAS RODs still has to be done, but this will not happen before the silicon readout development.

Minor modifications are needed to the reference timing circuit developed by SLAC to adapt the 476 MHz SLAC RF to the 400 MHz LHC RF, and to convert the 400 MHz stabilized clock to 40 MHz and interface it with the trigger board.

The location of the detectors close to the beam pipe but far from the ATLAS IP, requires a moderately radiation-hard pre-amplifier. Recent literature searches indicate that the rad hardness of the amplifier is not an issue: see "Proton Tolerance of InAs Based HEMT and DHBT Devices," by Steven M. Currie et al. 04077284 1-4244-0638-2/06/$20.00 02006 IEEE, for example, which observes no radiation damage up to 50 $\times 10^{12}$ p/cm^2 corresponding to 6.7 Mrads. The other components located in the alcove should not have significant radiation concerns assuming that the cable run to the alcove does not introduce an unacceptable level of jitter in the timing measurement (this will be tested this summer). If the jitter is appreciable, then the CFD would have to be located closer to the detector, and the CFD radiation tolerance would have to be evaluated, so we will preemptively study this as well. The mechanics, grounding, and shielding will have to be studied in detail based on the final choice of MCP-PMT, for initial studies we will use the default Photonis Planacon.

3.1 Goals and timescales for electronics R&D

This R&D effort is focussed on converting from a few channel prototype system to the final system, and adding new functionality in the form of an ADC, and a trigger circuit that is necessary to scale the clock rate and also can provide a first level trigger.

1. **Goal:** Develop amplifier board. Prototype has been build and is being tested at Stony Brook. **Timescale:** July 2011

2. **Goal:** Test radiation tolerance of amplifier board and CFD and improve as needed. **Timescale:** December 2011

3. **Goal:** Develop trigger circuit (Stony Brook). Currently in conceptual design stage. Second iteration of amplifier board based on test beam and UTA tests. **Timescale:** December 2011

4. **Goal:** Develop new HPTDC board (Alberta). Currently have schematic drawings. **Timescale:** December 2011

5. **Goal:** Final version of amplifier board and trigger circuit. **Timescale:** August 2012

6. **Goal:** Integrate final HPTDC board with ATLAS DAQ via RODs. **Timescale:** December 2012

7. **Goal:** Complete reference clock development. **Timescale:** December 2012

8. **Goal:** Grounding and shielding studies. **Timescale:** Spring 2013

Outlook:

We anticipate that the timing front-end electronics will be developed and tested by 2013 given sufficient funding, however, the U. S. funding situation has deteriorated recently. Some work is continuing without funds on the prototype amplifier board, and the next generation HPTDC board. The development of a full 8 channel prototype, including the trigger circuit, ADC, and reference clock, however, will not be possible unless there is support in a timely manner.