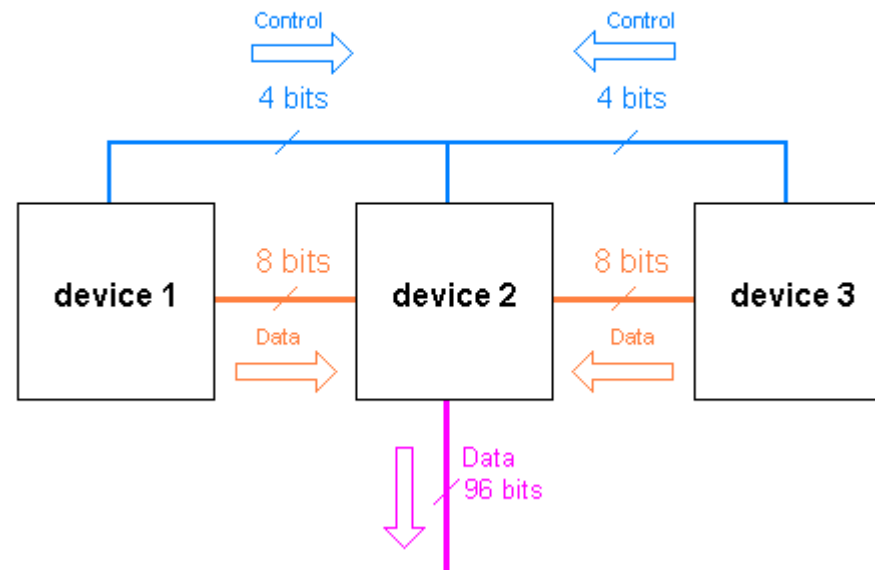
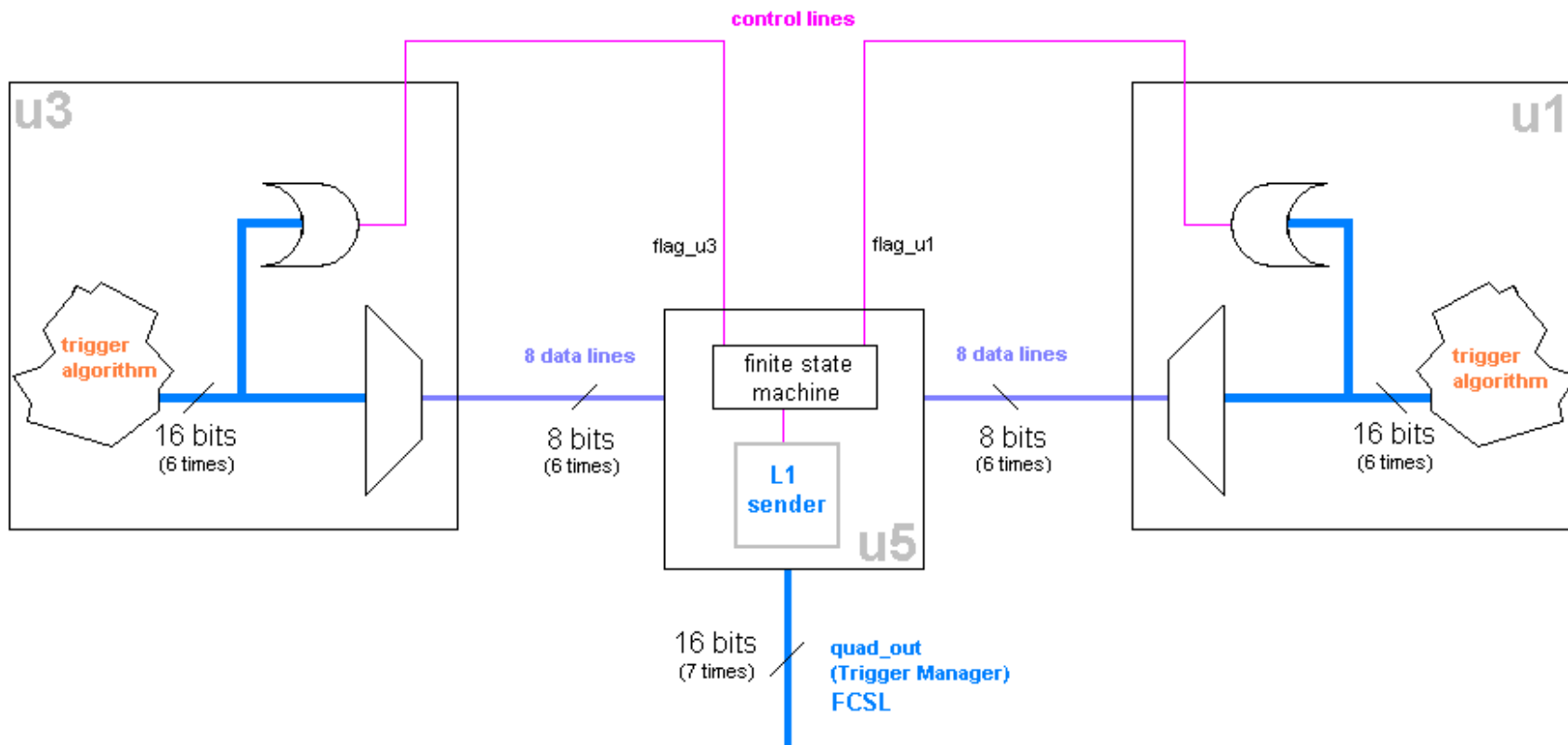


# Arbiter for DFE output bus

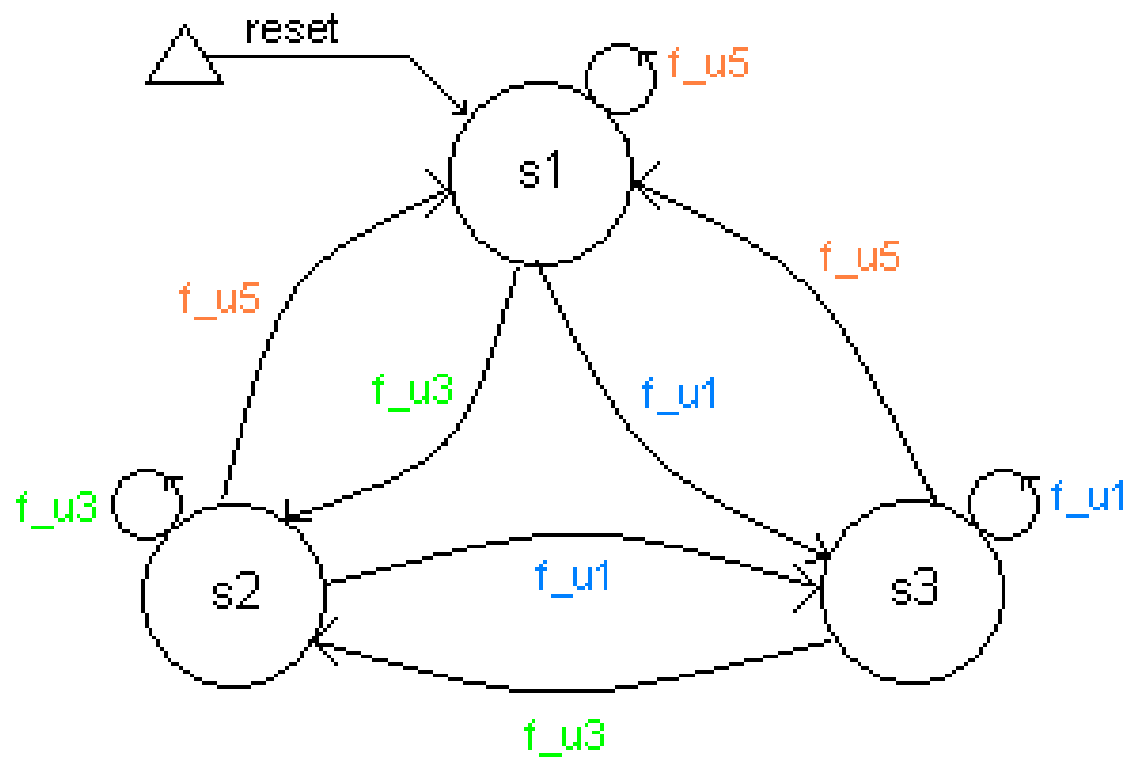
## Proposal # 2



# General Scheme



# Finite State Machine



State 1 -- sends results from U5

State 2 -- sends results from U3

State 3 -- sends results from U1



# Features with New Disposition

- 1. Multiplexer Speed.** The rising and falling edges of the clock have been used increasing the speed of the codification until the point in which it match the general input clock.
- 2. 16 bit wide data bus.** The results bus has been arranged in such a way that all the information from each frame (16 bits) is going to be passed to the L1Sender located in U5. The previous version just sent the result of the additions.
- 3. DFE output bus.** It will not show any problem for transmission instability, for U5 will drive the DFE output bus with no inference of the other two devices.
- 4. U5 Dependence.** The reliability of the DFE output will depend totally in the U5 L1 Sender. It could be negative in the case that U5 does not work as should be (verification through 1553, a *possible solution*)